ARC45: Dual Channel CCD Video Processor Board

This user's manual describes the ARC45 CCD video processor that is used in both Gen II and Gen III systems. It serves two functions - processing and digitizing the video outputs from the CCD and supplying DC bias voltages to the CCD. It contains two identical video processing circuits that simultaneously process and digitize signals from two CCD video outputs. Two 16-bit analog-to-digital (A/D) converters are provided on the board, each with a total sample and conversion time of one microsecond. Their digital outputs are multiplexed on the backplane on dedicated A/D data pins to the timing board for transmission to the host computer over the fiber optic data link. The DC bias supply section of the board provides ten low noise, digitally programmable voltage outputs with a variety of voltage ranges suitable for direct connection to CCDs, as well as two offset voltages for the two video processors. This board differs from the ARC41 video processing board in having a three op amp differential input circuit on each of the two video processors, as well as the single ended circuit of the ARC41, but without the option of DC coupling. A block diagram of the board is shown in Fig. 1. Some of the addresses and voltage ranges of the DC bias outputs have also been changed from the ARC41, but the timing and the signal processing technique have been preserved.

THEORY of OPERATION

The CCD output source signal, sometimes called CCD video, can be connected directly to the input DB9 connector, which should then have a load resistor connected to ground. The load resistors are mounted on fork terminals to enable the user to install and modify their values without damaging the board. This load resistor is normally NOT installed at the factory. Values of 20k are normally used for Loral and SITe sensors, and a value 6.8k and 5.0k have been used with the higher gain E2V devices.

The preamp needs to be jumper selected to be either AC coupled to the CCD or received differentially, typically over a long cable from a preamplifier located near the CCD. In AC coupling an 0.1µf capacitor is connected between the video signal and the non-inverting input of the preamplifier op amp to remove the large DC offset of the video signal. The preamp op amp selected is an Analog Devices AD829 which is a fast, low noise voltage feedback part, operated with a non-inverting gain of x4. At this gain it has a small signal bandwidth of 74 MHz, a slew rate of 70 volts per microsecond, an input voltage noise density of 1.7 nanovolts per root Hertz and an input current noise density of 1.5 picoamps per root Hertz. Although its input current noise density is larger than similar FET input parts its input voltage noise is much lower, so the output noise is lower when used with high gain CCDs that have output impedances up to several thousand kilohms.

The video signals are brought into the board on the DB15 connector with male pins, P1. The pinout is as follows:

TABLE 1 – DB15 Video Input Connector Pinout

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DB15 pin #    Function
    1         Single ended input, ch. A
    2         Differential input, non-inverting, ch. A
    3         Differential input, inverting, ch. A
    4         Preamp output, ch. A
    5         Preamp output, ch. B
    6         Differential input, inverting, ch. B
    7         Differential input, non-inverting, ch. B
    8         Single ended input, ch. A
    9         Ground
    10,14     Guard ring drive, not useful
    11, 12, 13, 15 Ground
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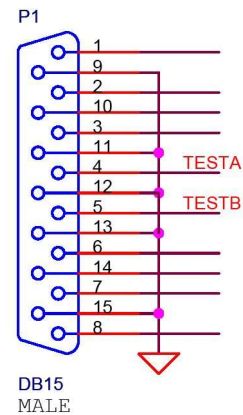
Following the preamp is a DC restore circuit whose
function is to maintain the average signal level so the op amps and analog switches are
within their normal operating ranges. The DC restore switch clamps the signal level to
ground every pixel before the signal is sampled.

The gain select stage has four software selections - x1.0, x2.0 x4.75 and x9.5, set by a
resistor ladder. The polarity select op amp simply inverts or buffers the signal to accomplish
the subtraction of (signal - baseline) which is proportional to the charge collected by the
CCD pixel. It is implemented by a differential amplifier with switchable resistors on the
input. The integrator is a conventional RC integrator, but with a choice of integration
speeds. With the 3.9 nf capacitor switched out the integrator has an RC time constant of
500 nanosec, so will have a gain of unity for this integration time. This setting is suitable
for operation in the fastest readout mode of 1.0 microsecond total processing time per pixel.
The 3.9 nf capacitor can be switched in for a slower integration suitable for slower readouts
where the stage will have unity gain for an integration time of 4.4 microsecond. The
integrate analog switch is closed to enable the integrator, and the reset integrator switch is
closed to discharge the integration capacitor(s) after each pixel is sampled. A simple x2
gain inverting stage follows the integrator and accepts an output offset voltage from a DAC
that allows a voltage to be subtracted from the signal before the A/D conversion. The A/D
converter is a fast 16-bit part that samples its input for 300 nanoseconds before its start A/D
signal goes high and requires another 700 nanoseconds before its digital output data is
valid. The digital output data are written to a latch when the XFER signal is clocked high,
and then transmitted over the backplane when the timing board asserts the appropriate A/D
selection lines, usually with the SXMIT command.

Some of the analog switches need to be switched every pixel, and are controlled by a simple
latch operating from the WRSS (write switch state) signal from the timing board that can be
updated every 40 nanoseconds. Other analog switches are rarely set and are controlled from
the serial data link from the timing board. The analog switches are all Siliconix DG611
parts with a low control logic input signal closing the switch. These are fast, low ON
resistance, and low charge dumping parts that unfortunately can be easily damaged if their
input voltage ranges are exceeded. This has necessitated the insertion of several protection
diodes in the circuit and the operation of the op amps driving the switches from
unconventional voltages, both to limit the voltage range on the switches and to lower power

dissipation. Both video processors on the same board have the same timing. These are the following -

TABLE 2 - Fast timing analog switch definition

Function	Schematic name	Timing	Description
Reset integrator	RESET	SS0	Low to reset the integrator
DC Restore	DC-REST	SS1	Low to DC restore
Polarity -	POL-	SS2	Low for inverting signal integration
Polarity +	POL+	SS3	Low for non-inverting signal integration
Integrate	INTEG	SS4	Low to integrate
Start A/D	A/D	SS5	Low to high transition to start A/D conversion
Transfer A/D	XFER	SS6	Low to high transition to transfer data from the A/D to a latch

Another set of analog switches are generally configured only during system initialization, and are controlled from serial words sent from the timing board, the same mechanism used to update DAC voltages. They can be set to different values on the two video processors, channels A and B. These are as follows -

TABLE 3 - Configuration analog switch definition

| Function	Schematic name	Data value	Description
Gain ch. A, x9.5	GAIN-A-0	D0	Low to enable x9.5 gain on ch. A
Gain ch. A, x4.75	GAIN-A-1	D1	Low to enable x4.75 gain on ch. A
Gain ch. A, x2.0	GAIN-A-2	D2	Low to enable x2.0 gain on ch. A
Gain ch. A, x1.0	GAIN-A-3	D3	Low to enable x1.0 gain on ch. A
Gain ch. A, x9.5	GAIN-B-0	D4	Low to enable x9.5 gain on ch. B
Gain ch. A, x4.75	GAIN-B-1	D5	Low to enable x4.75 gain on ch. B
Gain ch. A, x2.0	GAIN-B-2	D6	Low to enable x2.0 gain on ch. B
Gain ch. A, x1.0	GAIN-B-3	D7	Low to enable x1.0 gain on ch. B
Int. speed, Ch. A	INTEGRATE-A	D8	High for fast integrate speed, ch. A
Int. speed, Ch. B	INTEGRATE-B	D9	High for fast integrate speed, ch. B

The 12-bit DAC circuits for the DC bias supplies receive their digital data words over serial lines from the PAL U29 that converts 24-bit words from the timing board's synchronous serial interface (SSI) to 16-bit serial words routed to each DAC on the video board. Two of the DACs have bipolar outputs from +10 to -10 volts, and one of them has unipolar outputs from +2.5 to +10 volts. Ten outputs are passed through DG405 switches whose function is to be open whenever there is reason to suspect that the voltages are not set to their proper values or the power supply to the controller has failed. The control line TIM-D-ENCK, controlled by the timing board, is set high to close the switches and allow the DC bias voltages to propagate to the output connector. RC filters then decouple any remaining noise on the lines. The table of available voltages follows, where typical names are assigned to some of them.

TABLE 4 - DC bias voltages definition

DB25 pin #	Function	Voltage range	DAC address	Description
	Offset-A		$0C8xxx	Video Offset, Channel A
	Offset-B		$0CCxxx	Video Offset, Channel B
1	VOD-A	+7.5 to +30	$0D0xxx	Output Drain, ch. A
2	VOD-B	+7.5 to +30	$0D4xxx	Output Drain, ch. B
3	VRD-A	+5.0 to +20	$0C0xxx	Reset Drain, ch. A
4	VRD-B	+5.0 to +20	$0C4xxx	Reset Drain, ch. B
5		+7.5 to +30	$0D8xxx	
6		+7.5 to +30	$0DCxxx	
7		Ground		
8		Ground		
9	VOG1-A	-10 to +10	$0E0xxx	Output Gate #1, ch. A
10	VOG1-B	-10 to +10	$0E4xxx	Output Gate #1, ch. B
11	VOG2-A	-10 to +10	$0E8xxx	Output Gate #2, ch. A
12	VOG2-B	-10 to +10	$0ECxxx	Output Gate #2, ch. B
14		-15 volts regulated power		
15		+15 volts regulated power		
16		-6.5 volts raw power		
17		+6.5 volts raw power		
18		-5 volts regulated power		
19		+5 volts regulated power		
13,20,21,22,23,24,25	Ground			

BOARD LAYOUT and POWER REGULATION

The DC bias voltages are output on the large 25-pin DB connector at the lower left of the board following the pinout of Table 3. Power supply test points are provided near the regulators that generate them. The tolerances required by the A/D converter to operate within specifications are pretty tight: +/- 0.50 volts on the two fifteen volt supplies and +/- 0.25 volts on the two five volt supplies. There is an additional test point in the lower right hand corner of the board that connects to the digital five volts supply, which is not regulated on this or any other controller board.
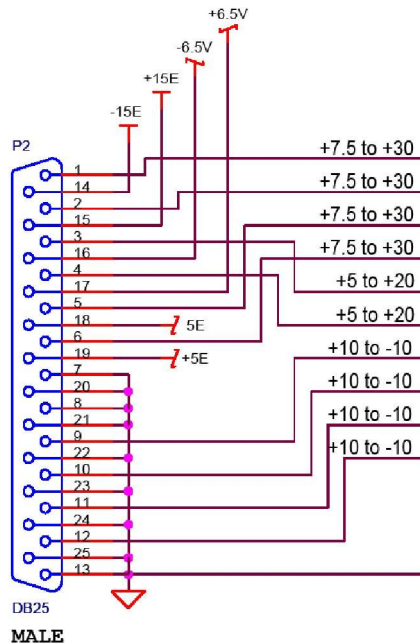
BOARD JUMPERING

Fig. 3 shows an enlargement of the jumpers that need configuring on the board. The parts layout of the preamp and input offset circuitry is shown on the left where the top channel jumpers for channel A are shown configuring the

preamp for AC coupling. The lower channel B is shown configured for DC coupled operation. For ease of setup the default jumpers are put in the AC coupled mode.

The ground jumper JP9 that is used to connect the analog and digital grounds planes on the board is shown in the figure. Lower readout noise has been found in prototype systems with the jumper installed, and on many boards this jumper is not installed but rather a wire is soldered in place of R92 right next to it. The user may cut the wire in R92 at will to break the connection between digital and analog ground planes if desired, and install a jumper header in JP9 to easily switch back and forth to determine the minimum noise configuration. The jumpers JP20 and JP21 select between obtaining the power for the +/- 5 volts regulated supplies from either +/-16.5 volts (jumpers on bottom) or from +/-6.5 volts (jumpers on top).

The board addressing jumpers JP1 to JP8 determine the addresses of the DACs, A/D converters and timing switches. The four jumpers on the left side, JP1 to JP4 in the schematic, labeled DAC-A/D 0 to 3 on the silk screen layer on the board, determine the board address for reading the contents of the two A/D converters and for setting the value of the DACs. An un-installed jumper will be read as a zero, and an installed jumper will be read as a one. The four jumpers set the address of the four most significant bits of the five addressing bits allowed in a system, with the least significant bit selecting the A (bit D0 = 0) or B (bit D0 = 1) channel. A maximum of sixteen video processing boards may be installed in a system. As discussed in the timing board user's manual, the A/D counts may be read with the SXMIT command, possibly on several different boards, and transmit them as a series to the host computer, bypassing the timing board DSP entirely. The example below describes several different jumper settings -

TABLE 5 – A/D Addressing examples

JP1	JP2	JP3	JP4	SXMIT	Comment
OFF	OFF	OFF	OFF	$00F000	Only read the first A/D, board 0
OFF	OFF	OFF	OFF	$00F041	Only read the second A/D, board 0
OFF	OFF	OFF	OFF	$00F040	Read both A/Ds from board 0
ON	OFF	OFF	OFF	$00F062	Read both A/Ds from board 1

And several examples for more than one A/D board:

JP1	JP2	JP3	JP4	SXMIT	Comment
OFF	OFF	OFF	OFF	$00F0C0	Read four A/Ds, boards 0 and 1
ON	OFF	OFF	OFF		
OFF	ON	OFF	OFF	$00F1C4	Read four A/Ds, boards 2 and 3
ON	ON	OFF	OFF		
OFF	OFF	OFF	OFF	$00F7C0	Read 32 A/D, boards 0 to 3
ON	OFF	OFF	OFF		
OFF	ON	OFF	OFF		
ON	ON	OFF	OFF		

The jumpers JP1 to JP4 also select the board address when the timing board writes to the DACs. The DAC and A/D board addresses are always the same, and there is one set of DACs per video board addressed from one jumper setting, allowing for a maximum of 16 video processor boards per system. The most significant bits D20 to D24 of the serial word written out over the backplane pins TIM-A-STD match the jumpers JP1 to JP4 to select the video processor board to be written to, and the bits D14-D17 select which of the four DACs on a board and which of each of its internal four DAC addresses is addressed, following Table 3 above. Bits D18 and D19 must be high to select a video processing board, while if they are not both high a clock driver DAC is addressed.

The four jumpers on the right side JP5 to JP8 in the schematic, labeled switch 0 to 3 on the silk screen layer, determine the address that the fast timing analog switches will respond to. Generally all the video boards in a system are have the same timing jumpers and have the same timing, though 16 timing addresses are provided. The supplied DSP code always sets the video board timing address to zero, and none or the four jumpers are installed.

Selection of the single ended or differential inputs to the board is made with the three prong header block near the front of the board. Putting a jumper between the upper and middle header pin selects the single-ended amplifier stage.